ECE 8455 Advanced Digital Design Using FPGAs

Fall 2020

Instructor: Dr. Xiaofang Maggie Wang (xwang@villanova.edu)
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Credits: 3

Lectures: Wednesdays, 12 p.m. – 2:30 p.m., live through Zoom. Videos will be posted by the end of the day.

Office Hours: TR 2:30 pm – 3:30 pm through Zoom or by appointment

Course Web: We will be using the Blackboard (BB) to organize learning materials. The class contents homepage will be constantly updated with lecture slides and videos, assignments, readings, references, etc. You are required and assumed to check the homepage regularly for up-to-date information.

Textbook: There is no particular textbook as I will be integrating materials from many sources. However, a comprehensive VHDL reference book is required. If you do not have one, the following book is recommended.

A VHDL Primer, **3rd edition,** J. Bhasker, Prentice Hall, 1999, ISBN: 0-13-096575-8.

References: 1. *Advanced FPGA Design*: Architecture, Implementation, and Optimization, by *S. Kilts*
2. Many documents on the course **References** web page

Required Background: Digital logic design and VHDL basics (VU ECE 2044 & ECE 2045 or equivalent courses).

Course Overview

An FPGA (Field-Programmable Gate Array) device is a semi-custom integrated circuit (IC) that contains an array of programmable (configurable) logic blocks and programmable (configurable) interconnects that connect the logic blocks. FPGAs have undergone phenomenal advances since its introduction in the mid-1980s, especially during the last few years. Such advances, along with the skyrocketing costs of nano silicon processes and the ever-shrinking time-in-market window continue to successfully help FPGAs erode ASIC and ASSP market shares.

The objective of this course is to introduce students to advanced digital design using VHDL/Verilog for FPGAs. We start with

fundamental concepts of FPGAs and focus on practical issues of FPGA-based digital design later on. Students will learn various FPGA design approaches, such as HDL-, schematic-, and C/DSP-based methods. The final segment of the class covers special topics that identify current trends in FPGA technologies. The design and implementation tools used throughout the course include Quartus Prime and ModelSim. Practical experience is gained by implementing various designs and a comprehensive project on the Intel (Altera) FPGA development board. Please check the following course schedule of topics.

Grading Policy

1. Homework Assignments -- 50%
2. Final exam -- 25%
3. Project: 25%

Planned Schedule

(Check the BB homepage for lecture slides, videos, in-class demos, readings, assignments, etc.)

Meeting	Topics
08/19	Course Overview; Introduction to FPGAs
08/26	FPGA design methodology and tools; *Quartus Prime Tutorial 1*
09/02	VHDL 1: Hardware modeling basics; Tutorial: *Basic ModelSim simulation*
09/09	Introduction to Verilog
09/16	VHDL 2: Behavior modeling
09/23	VHDL 3: FSM and advanced topics
09/30	Testbench; Design Examples: Audio codec & VGA controller Advanced ModelSim simulation
10/07	Memory designs for FPGA-based systems; Partial reconfiguration
10/14	VHDL/Verilog codling style for synthesis optimizations
10/21	Optimizing performance by driving FPGA synthesis tools
10/28	Lab time; Project help
11/04	FPGA reset and clock circuits and timing issues; Command Line Scripting
11/11	FPGA Power Analysis and Optimization
11/18	Final exam

About Self-Guided Learning

Learning how to look for appropriate technical documentation, read and understand them efficiently in a focused manner is one of the essential engineering skills, and one of the objectives of the course. You are expected to look for appropriate documentation, mostly through vendor's website, when you have questions and problems with the assignments and project. In addition to the lectures, additional reading assignments will be posted on the course web as needed.

Attendance and Participation

You are expected to attend all the class meetings and are responsible for all the material covered in class including handouts and class notes. In-class students should inform the instructor if they plan to be late or absent from class. In all cases, students should be prepared to provide documentation to petition for *excused* absences to the appropriate Associate Dean. The form for requesting an *excused* absence can be found here (http://www1.villanova.edu/villanova/engineering/resources/policies/forms/studentAbsence.html). Absence from class does not release the student from work assigned. Students who miss an in-class obligation (exam, presentation, etc.) due to an excused absence will not be penalized - the instructor may offer a make-up test, arrange an alternative time for a presentation, exempt a student from the assignment, or provide another arrangement.

Adherence to the Student Code of Conduct and the CARITAS Commitment

Students are expected to act in a professional and respectful manner to their fellow students, faculty, and staff. Students should become acquainted with and understand the responsibilities set forth in the Student Handbook, especially those in the sections on Policy and Regulations. Adherence to University regulations is expected and required for successful completion of the program of studies. Enforcement within the classroom of policies regarding classroom behavior is the responsibility of the faculty member. All other discipline problems are to be referred to the Dean of Students.

Students, faculty, and staff are expected to comply with the CARITAS Commitment. Students should wear masks, practice social distancing and good hygiene, wipe down their work area upon arrival and departure, and request an excused absence if they are not feeling well.

Academic Integrity

The College of Engineering is committed to creating an environment of academic integrity and ethical decision-making that we hope is reflected in the actions of our students and graduates. As Villanova students, integrity is central to the University mission. As engineers, our code of conduct requires us to place honor and integrity at the forefront of everything we do. As engineering students, it is expected that you will begin to adopt these values and instill them into your work habits. Students violating the academic integrity policy will receive a zero on that assignment or exam and the violation will be reported to the Associate Dean for Academic Affairs.

The University's academic integrity policy can be found here:
https://www1.villanova.edu/villanova/provost/resources/student/policies/integrity.html.
The College of Engineering has adopted the following exam guidelines:

- Students must arrive before the start of the exam. Under exceptional circumstances a student may need to arrive late, but he/she can enter the exam no later than 5 minutes after the start of the exam.
- All cell phones must be turned off and stored away until the student exits the exam room.
- The official Villanova class attendance policy must be followed when requesting excuses for absences or lateness to an exam.
- Each student must write and sign the following statement, "*I have neither given nor received any unauthorized assistance in the completion of this exam.*"

Academic Accommodations for Students with Disabilities

It is the policy of Villanova to make reasonable academic accommodations for qualified individuals with disabilities. If you are a person with a disability please contact me after class or during office hours to make arrangements.
If you have a non-physical disability you need to register with the Learning Support Office by contacting 610-519-5176 or at learning.support.services@villanova.edu as soon as possible. Registration is needed to receive accommodations.
The Office of Disability Services collaborates with students, faculty, staff, and community members to create diverse learning environments that are usable, equitable, inclusive and sustainable. The ODS provides Villanova University students with physical disabilities the necessary support to successfully complete their education and participate in activities available to all students. If you have a diagnosed disability and plan to utilize academic accommodations, please contact and register with Gregory Hannah, advisor to students with disabilities @ 610-519-3209 or visit the office on the second floor of the Connelly Center.

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